This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

A New Standby Structure Integrated with Boost PFC Converter for Server Power Supply

Jae-Il Baek, *Member*, *IEEE*, Jae-Kum Kim, *Member*, *IEEE*, Jae-Bum Lee, *Member*, *IEEE*, Moo-Hyun Park, *Student Member*, *IEEE*, and Gun-Woo Moon, *Member, IEEE*

***Abstract*— In the standby stage of a server power supply, the flyback converter has been widely used due to its simple structure and low cost. However, since the flyback converter suffers from high voltage stress and a large transformer, it degrades the efficiency and power density of the server power supply. To relieve these drawbacks, this paper proposes a new standby structure where a flyback converter is integrated with a boost PFC converter. The proposed standby structure can relieve the high voltage stress and eliminate the large transformer of the conventional flyback converter because the primary side of the flyback converter is merged with the boost PFC converter. Thus, the proposed structure can achieve high efficiency and high power density in the standby stage. Furthermore, it can help the boost PFC converter achieve a soft switching operation, which results in a high-efficiency PFC stage. As a result, the proposed structure improves the overall efficiency and power density of the server power supply. The validity of the proposed structure is confirmed by a prototype with 100-240V_{rms} AC input, 750W PFC output, and 12V/2A standby output.**

***Index Terms*— Boost PFC converter, flyback converter, PFC stage, server power supply, soft switching, standby stage.**

I. INTRODUCTION

RECENTLY, as the internet traffic has increased all over the world, the data center market has consistently grown. Accordingly, the server power supply for the data center has also been developed actively. In general, the server power supply requires high efficiency under heavy load conditions because it operates under heavy loads during the day. Moreover, since the server power supply runs under light load conditions at night and dawn, the light load efficiency has also become important in the server power supply market [1]. This tendency is confirmed by the 80 PLUS incentive program [2], which requires high efficiency from 10% to 100% load conditions in the normal mode where the server power supply mostly operates. Furthermore, the server power supply needs high power density to meet the demand of miniaturization of the power supply. Therefore, high efficiency and high power density are essential in the server power supply.

Manuscript received May 5, 2018; accepted August 28, 2018. This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2018R1A6A3A01012753).

Jae-Il Baek, Moo-Hyun Park, and Gun-Woo Moon are with the School of Electrical Engineering in the Korea Advanced Institute of Science and Technology, Daejeon 34141, Republic of Korea (e-mail: dpi1067@kaist.ac.kr; moohyun3@kaist.ac.kr, and gwmoon@kaist.ac.kr).

Jaek-Kuk Kim is with Solu-M, Yongin-si 16914, Republic of Korea (e-mail:fred.kim@solu-m.com

Jae-Bum Lee is with Korea Railroad Research Institute (KRRI), Uiwang-Si 16105, Republic of Korea (e-mail:leejb83@krri.re.kr)

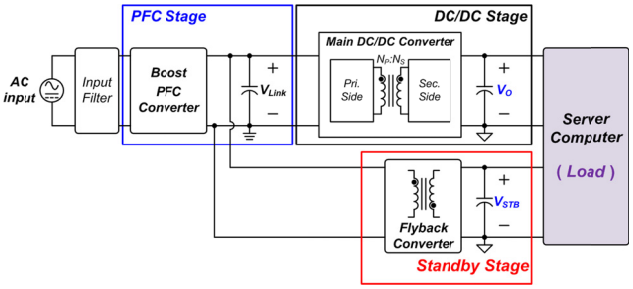

Fig. 1. General structure of server power supply.

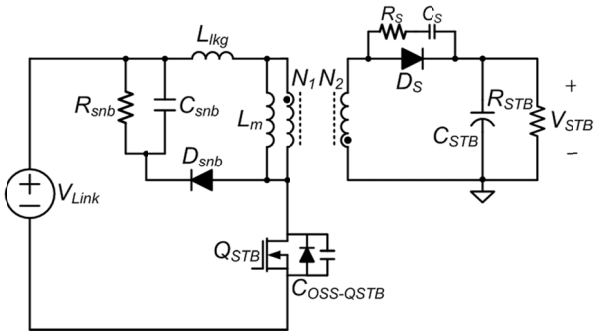

Fig. 2. Circuit diagram of conventional flyback converter.

As shown in Fig. 1, the server power supply is typically divided into three stages to regulate the main output voltage (V_O) and standby output voltage (V_{STB}): 1) a power factor correction (PFC) stage, 2) a main DC/DC stage, and 3) a standby stage. In the PFC stage, a continuous conduction mode (CCM) boost PFC converter is normally used to comply with the harmonics regulation and achieve a small conduction loss for medium-to-high power applications [3]-[5]. The main DC/DC stage, following the PFC stage, regulates V_O precisely. Finally, the standby stage is used to regulate V_{STB}. When the server power supply is in the standby mode, V_{STB} is only regulated to supply the standby power to the server components for the service processor and server boots. On the other hand, in the normal mode, all stages have to operate to provide both V_O and V_{STB}. Therefore, in the normal mode requiring high efficiency, the total efficiency of the server power supply is affected by the standby stage as well as the PFC and DC/DC stages. As a result, the standby stage should obtain high efficiency in the normal mode to achieve a high-efficiency server power supply.

Typically, the standby power is less than 30W. Thus, the flyback converter is widely adopted in the standby stage considering the power density and cost, as shown in Fig. 2 [6]-[11]. However, the flyback converter has lower efficiency than the other two stages (PFC and DC/DC stages) because of its

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

large power loss in the primary side [9]-[12], which degrades the efficiency of the server power supply over all the load conditions [9]-[11]. First, since the switch (Q_{STB}) in the flyback converter suffers from high voltage stress and hard switching operation, Q_{STB} causes a large switching loss. Second, the primary RCD snubber results in a large power loss due to high voltage stress and additional voltage spike caused by the resonance between the leakage inductor of the transformer (L_{lkg}) and the output capacitor of Q_{STB} ($C_{OSS\text{-}QSTB}$). Furthermore, it has a large transformer because of the dc-offset magnetizing current in the transformer [13]. Therefore, the flyback converter also degrades the power density of the server power supply.

For those reasons, many approaches have been proposed to improve the efficiency and power density of the flyback converter [9]-[12]. In [9], the secondary side of the flyback converter was integrated into that of a multi-output PSFB converter with one additional switch. This method regulated V_{STB} through the operations of the PSFB converter and the additional switch instead of the primary side of the flyback converter. Thus, it eliminated the power loss caused by the primary side of the flyback converter. However, the method proposed in [9] caused additional conduction loss in the PSFB converter so it has limitations in achieving a high-efficiency server power supply. Moreover, in the standby mode, since V_{STB} needs to be regulated without the operation of the PSFB converter, this structure still has to utilize the primary circuit and large transformer of the flyback converter. Thus, this approach degrades the power density and increase the cost due to the large transformer and the additional switch. In [10], the primary side of the two-switch flyback converter was combined with that of the PSFB converter by sharing the lagging leg switches of the PSFB converter. In the normal mode, the structure proposed in [10] achieved high efficiency by removing the RCD snubber loss and obtaining the ZVS operation of primary switches without additional components. However, this structure also increases the conduction loss of the PSFB converter and still has a large transformer of two-switch flyback converter, which results in a low power density. Next, in [11], the output of the flyback converter was merged with that of the PSFB converter using an ORing diode. In the normal mode, since the PSFB converter that is highly efficient is only used to regulate V_O and V_{STB}, the power loss of the primary side in the flyback converter can be eliminated. However, this structure cannot eliminate any component of the flyback converter to provide V_{STB} in the standby mode. Furthermore, two additional diodes are required to integrate outputs of the flyback converter and PSFB converter. Above all, this structure can only be applied to applications requiring the same V_O and V_{STB}. Meanwhile, another study focused on the flyback converter itself. In [12], the resonant operation was applied to the flyback converter to achieve the soft switching operation of the primary switch. That approach increased the switching frequency with a small switching loss, which enabled the flyback converter to reduce its transformer size. However, the structure proposed in [12] also requires an additional diode and has the RCD snubber loss and switching loss.

Meanwhile, to achieve high efficiency and high power density, integrating the boost PFC converter and flyback converter can be also good approach [14]-[16]. In [14], the boost PFC and flyback converters were integrated to eliminate the flyback switch. Moreover, the converter proposed in [14] reduced the RCD snubber loss by adopting lossless snubber. However, it suffers from the hard switching operation and requires two magnetic cores and additional diode, which results in a low efficiency and low power density. The converter proposed in [15] achieved high power density by eliminating one magnetic core. In addition, it obtained the soft switching operation of all switches without additional components. Nevertheless, this converter has limitation in obtaining high efficiency because it requires small boost inductance to achieve the soft switching operation. Above all, the converters proposed in [14] and [15] cannot be applied to the server power supply because they are not able to regulate V_O and V_{STB}, simultaneously. Meanwhile, the converter proposed in [16] can regulate V_O and V_{STB} despite of the integration. Besides, by combining the active snubber inductor and flyback transformer, it minimized the switching loss of the boost PFC stage and losses of the active snubber cell, which leads to high efficiency. However, this approach still has to use two magnetic core and RCD snubber. Moreover, it requires active snubber cell composed of a diode and switch to obtain the soft switching operation. Therefore, the converter proposed in [16] also has a limitation in achieving a high power density.

In this paper, a new standby structure is proposed to achieve a high-efficiency and high-power-density server power supply. The proposed standby structure can be effectively derived by integrating the primary side of the flyback converter with the boost PFC converter. The proposed standby structure has three desirable features that make it superior to the conventional standby structure, which is composed of the boost PFC converter and flyback converter. First, since the boost PFC converter is used as the primary side of the flyback converter, the proposed structure relieves high voltage stress and eliminates the RCD snubber. Second, the transformer of the flyback converter is able to be removed by integrating it with the boost inductor. Finally, the proposed structure achieves the soft switching operation of the boost PFC converter through the interaction of the integrated structure of the boost PFC and flyback converters. As a result, the proposed structure achieves high efficiency and high power density for the server power supply without any additional components. The analysis, design consideration, and experimental results of the proposed structure are discussed in the following sections.

II. Analysis of Proposed Standby Structure

A. Circuit configuration

Fig. 3 shows the circuit diagram of the conventional standby structure. This figure shows that the boost PFC converter is used for the PFC stage, and it is composed of an input filter capacitor (C_{in}) for EMI noise, a boost inductor (L_B), a boost switch (Q_B), and a link capacitor (C_{Link}). Moreover, the synchronous rectifier switch (Q_S) can be used in place of the SiC diode due to the advancement of wide-band gap devices, such as SiC MOSFET and GaN FET, which results in higher efficiency by reducing the conduction loss [17]-[18]. Next, in the standby stage, the flyback converter is used and it consists

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

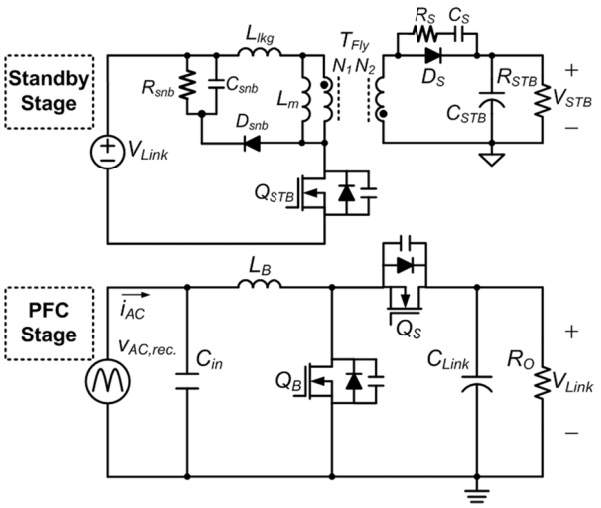

Fig. 3. Circuit diagram of conventional standby structure.

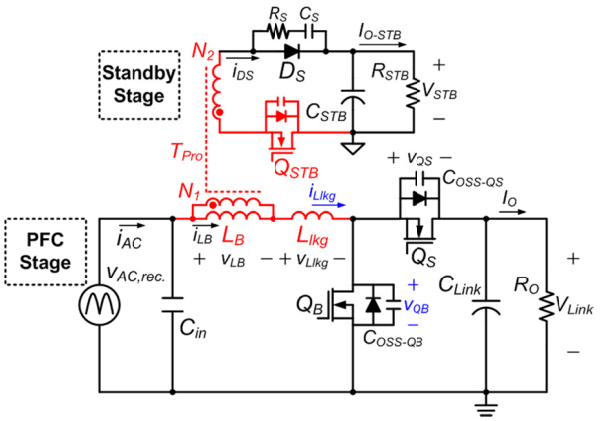

Fig. 4. Circuit diagram of proposed standby structure.

of the primary switch (Q_{STB}), the RCD snubber for clamping the voltage stress of Q_{STB}, the transformer (T_{Fly}), which has a magnetizing inductor (L_m) and a leakage inductor (L_{lkg}), a single-ended rectifier, and an RC snubber to limit the voltage stress of D_S [13].

Fig. 4 shows the circuit diagram of the proposed standby structure. In the proposed structure, since the primary side of the flyback converter is combined with the boost PFC converter, the proposed structure has three desirable features compared to the conventional one. First, in the PFC stage, the conventional boost inductor (L_B) is replaced with a boost transformer (T_{Pro}) to integrate L_B and T_{Fly}. Thus, the proposed structure effectively eliminates T_{Fly} only by adding a secondary winding (N_2) to L_B. Second, in the standby stage, Q_{STB} of the conventional flyback converter is moved into the secondary side. Thus, the proposed structure can considerably reduce the voltage stress on Q_{STB} compared to the conventional one because V_{STB} is much smaller than V_{Link}. Moreover, since the voltage stress on Q_{STB} can be damped by the RC snubber of D_S, the proposed structure is able to remove the conventional RCD snubber. Finally, the proposed standby structure can achieve the soft switching operation of the PFC stage through the energy transfer between the PFC and standby stages. As a result, the proposed structure can improve

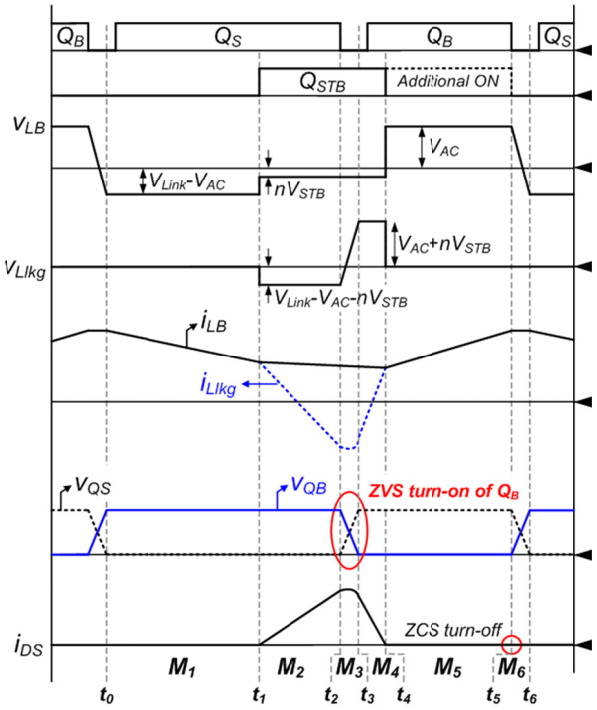

Fig. 5. Operational key waveforms of proposed standby structure.

the efficiency and power density without any additional components.

B. Operational principles

Figs. 4 and 5 show the circuit diagram and key waveforms of the proposed standby structure, respectively. As shown in Fig. 5, Q_B and Q_S are complementarily controlled to regulate the input current (i_{AC}) and V_{Link} like the conventional boost PFC converter. Q_{STB} is controlled to regulate V_{STB} like the conventional flyback converter. Moreover, Q_{STB} is turned on near the end of the ON state of Q_S to achieve the ZVS operation of Q_B, and simultaneously turned off with Q_B not only to obtain the ZCS turn-off operation of Q_{STB} but also to simplify the control of Q_{STB}.

***Mode 1* [t_0-t_1]:** At time t_0, the voltage across C_{OSS-QS} (v_{QS}) becomes zero so the current of L_B (i_{LB}) flows through the body diode of Q_S. Thus, the ZVS operation of Q_S is achieved. Then, i_{LB} starts to decrease because the voltage across L_B (v_{LB}) is V_{AC}-V_{Link}. i_{LB} can be given by

$$i_{LB}(t) = i_{Llkg}(t) = i_{LB}(t_0) - \frac{V_{Link} - V_{AC}}{L_B}(t - t_0). \quad (1)$$

where i_{Llkg} is the current of L_{lkg}.

During this mode, although v_{LB} has a negative value, the power cannot be transferred from the PFC stage to V_{STB} because Q_{STB} is turned off. Therefore, the proposed structure operates like a conventional boost PFC converter in this mode.

***Mode 2* [t_1-t_2]:** When Q_{STB} is turned on at t_1, the secondary diode (D_S) is put into operation. Thus, the voltage reflected from the secondary side is inversely applied to L_B. The equivalent circuit reflected to the primary side of this mode is as depicted in Fig. 6(a). In this figure, the voltage across L_{lkg}

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

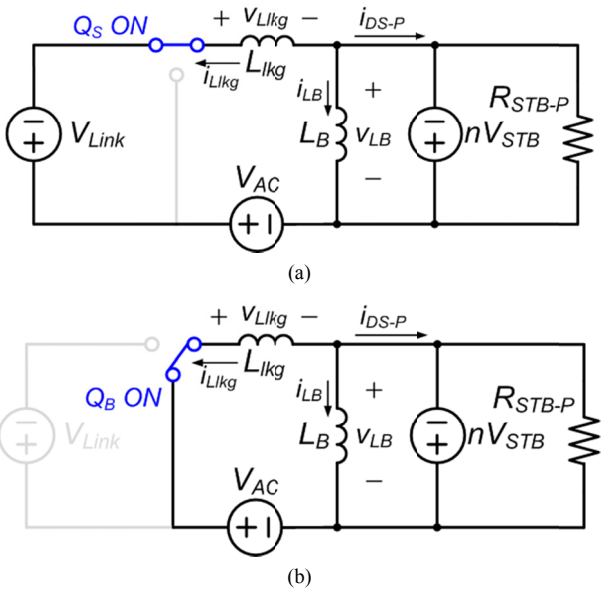

Fig. 6. Equivalent circuit reflected to primary side. (a) In mode2. (b) In mode. 4.

(v_{Llkg}) becomes V_{AC}+nV_{STB}-V_{Link} and v_{LB} is -nV_{STB}. Therefore, i_{Llkg} and i_{LB} can be separated, and the difference between them is transferred into i_{DS}. i_{Llkg}, i_{LB}, and i_{DS} can be expressed as follows:

$$i_{LB}(t) = i_{LB}(t_1) - \frac{nV_{STB}}{L_B}(t - t_1), \tag{2}$$

$$i_{Llkg}(t) = i_{LB}(t_1) - \frac{(V_{Link} - V_{AC} - nV_{STB})}{L_{lkg}}(t - t_1), \tag{3}$$

$$i_{DS}(t) = -ni_{DS-P} = n(i_{LB}(t) - i_{Llkg}(t)), \tag{4}$$

where n is the turns-ratio of the transformer (T_{Pro}), i.e., N_1/N_2, and $i_{DS\text{-}P}$ is the reflected i_{DS} to the primary side.

In (3), as i_{Llkg} decreases, it is able to have a negative direction at the turn-off state of Q_S, i.e., t_2. In addition, when Q_{STB} is turned on at t_1, since the initial current of Q_{STB} is zero, the ZCS turn-on of Q_{STB} can be achieved like the conventional flyback converter that operates with the discontinuous-conduction-mode.

***Mode 3* [t_2-t_3]:** At time t_2, Q_S is turned off. However, unlike the conventional boost PFC converter, since the current direction of i_{Llkg} is negative, the body diode of Q_S is not conducted. Thus, the reverse recovery problems caused by the body diode of Q_S are eliminated in the proposed structure. Moreover, because a negative i_{Llkg} is flow through $C_{oss\text{-}QB}$ and $C_{oss\text{-}QS}$, v_{QB} and v_{QS} can be discharged and charged by the energy stored in L_{lkg}, respectively.

***Mode 4* [t_3-t_4]:** At time t_3, v_{QB} becomes zero, and then i_{Llkg} flows through the body diode of Q_B. Thus, the ZVS operation of Q_B can be achieved unlike with the conventional boost PFC converter. Moreover, in Fig. 6(b), since v_{Llkg} is (V_{AC}+nV_{STB}), i_{Llkg} increases as follows:

$$i_{Llkg}(t) = i_{Llkg}(t_3) + \frac{(V_{AC} + nV_{STB})}{L_{lkg}}(t - t_3). \tag{5}$$

Meanwhile, i_{LB} decreases continuously like (2), and the power is still transferred from the PFC stage to V_{STB} until i_{Llkg} meets i_{LB}. This mode ends when D_S is turned off and reverse biased.

***Mode 5* [t_4-t_5]:** At time t_4, since D_S is reverse biased, the additional ON state of Q_{STB} has no impact on the operation of the PFC stage. Thus, i_{LB} and i_{Llkg} start to increase like in the conventional boost PFC converter. i_{LB} and i_{Llkg} can be expressed as follows:

$$i_{LB}(t) = i_{Llkg}(t) = i_{LB}(t_4) + \frac{V_{AC}}{L_B}(t - t_4). \tag{5}$$

***Mode 6* [t_5-t_6]:** When Q_{STB} and Q_B are turned off at t_5, there is no current flow at Q_{STB} unlike in the conventional flyback converter. Thus, Q_{STB} can achieve the ZCS turn-off operation, which leads to a small turn-off switching loss compared to the conventional one. In addition, v_{QS} and v_{QB} are discharged and charged by the energy stored in L_B. This mode ends when v_{QS} is zero.

C. Voltage gain

The voltage gain of the proposed standby structure can be obtained from the operational principles in Section II-B and Fig. 5. Assuming that the duration of *Mode 3* and *Mode 6* are negligibly short, the voltage-second balance across L_B and L_{lkg} can be expressed as in (7) and (8). Moreover, since the average current of i_{DS} is equal to $I_{O\text{-}STB}$, it can be given by (9).

$$(V_{Link} - V_{AC})D_A + nV_{STB}D_{STB} = V_{AC}(D_B - D_X), \tag{7}$$

$$(V_{Link} - V_{AC} - nV_{STB})(D_{STB} - D_X) = (V_{AC} + nV_{STB})D_X, \tag{8}$$

$$\frac{1}{2}D_{STB} \times \frac{n(V_{Link} - V_{AC} - nV_{STB})}{L_{lkg}}(D_{STB} - D_X)T_S = I_{O-STB}, \tag{9}$$

where D_{STB} is the duty ratio of Q_{STB} except for the additional ON time, D_B is the duty ratio of Q_B, D_A is the duty ratio of Mode 1(=1-D_B-D_{STB}+D_X), D_{STB}-D_X is the duty ratio of Mode 2, D_X is the duty ratio of Mode 4, D_B-D_X is the duty ratio of Mode 5, and T_S is the switching period.

Consequently, D_X and D_{STB} are derived from (7), (8), and (9) as follows:

$$D_X = \frac{D_{STB}(V_{Link} - V_{AC} - nV_{STB})}{V_{Link}}, \tag{10}$$

$$D_{STB} = \sqrt{\frac{2I_{O-STB}L_{lkg}V_{STB}}{nT_S(V_{Link} - V_{AC} - nV_{STB})(V_{AC} + nV_{STB})}}. \tag{11}$$

By substituting (10) and (11) for (7), the voltage gain of the proposed PFC stage is obtained as follows:

$$V_{Link} = \frac{V_{AC}}{1 - D_B}. \tag{12}$$

As can be seen in (12), the voltage gain of the proposed PFC stage is the same as that of the conventional CCM boost PFC converter [19]. Therefore, it is noted that the proposed

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

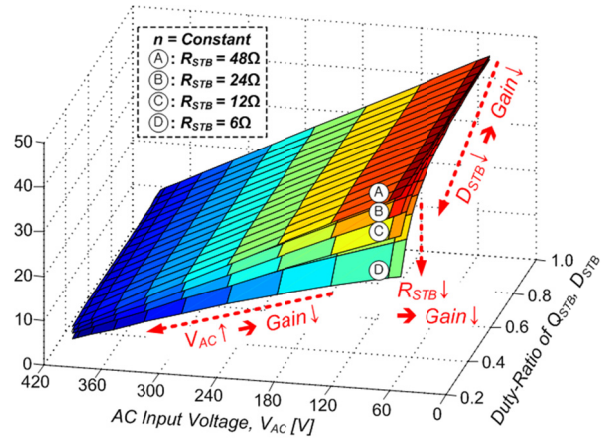

Fig. 7. V_{STB} of proposed standby stage according to V_{AC}, D_{STB}, and R_{STB}.

PFC stage can be designed and controlled like the conventional CCM boost PFC converter.

Meanwhile, the voltage gain of the proposed standby stage can be derived by substituting (10) and (11) for (8) as follows:

$$V_{STB}=\frac{V_{Link}}{n}\left[\left(\frac{1}{2}-\frac{V_{AC}}{V_{Link}}\right)-\frac{A}{D_{STB}^2}+\sqrt{\frac{1}{4}+\frac{A}{D_{STB}^2}\left(\frac{A}{D_{STB}^2}-1+\frac{V_{Link}}{V_{AC}}\right)}\right], \quad (13)$$

where A is $L_{lkg}/(n^2T_SR_{STB})$ and R_{STB} is the output resistor of the standby stage.

Using (13), V_{STB} of the proposed standby stage can be obtained according to V_{AC}, D_{STB}, and R_{STB}, as shown in Fig. 7. In this figure, it is seen that V_{STB} decreases as D_{STB} decreases or V_{AC} increases because the amount of power delivered to V_{STB} is determined from *Mode 2* to *Mode 4* in Fig. 5. Moreover, V_{STB} decreases as R_{STB} decreases. As a result, the proposed standby stage should be designed at the highest V_{AC} and the smallest R_{STB}, i.e., largest $I_{O\text{-}STB}$, because converters are generally designed to meet the output voltage requirement at the worst input and output conditions, which will be explained in Section III.

D. Voltage stress on semiconductor device

In this part, we discuss the voltage stresses on semiconductor devices in the conventional and proposed standby structures. In case of Q_B and Q_S, the voltage stresses are clamped to V_{Link} both in the conventional and proposed standby structures. On the other hand, since Q_{STB} in the proposed structure is located at the secondary side, the proposed structure has a different voltage stress from the conventional one as follows:

$$V_{QSTB-Conv}=V_{Link}+nV_{STB}, \quad (14)$$

$$V_{QSTB-Pro}=(V_{Link}-V_{AC})/n-V_{STB}, \quad (15)$$

where $V_{QSTB\text{-}Conv}$ and $V_{QSTB\text{-}Pro}$ are voltage stresses on Q_{STB} in the conventional and proposed standby structures, respectively.

In (14) and (15), $V_{QSTB\text{-}Pro}$ can be much smaller than $V_{QSTB\text{-}Conv}$ because (V_{Link}-V_{AC}) is divided by n as well as subtracted by V_{STB}. Thus, the proposed structure relives the problems caused by high voltage stress of the conventional Q_{STB}.

TABLE I
KEY DIFFERENCES BETWEEN CONVENTIONAL AND PROPOSED STANDBY STRUCTURES

	Conventional Structure	**Proposed Structure**
Control	Independent control of Q_{STB} and Q_B	Synchronization control of Q_{STB} and Q_B
Magnetic core#	2	1
RCD snubber	O	X
Q_{STB}	High voltage stress (ZCS turn ON)	Low voltage stress (ZCS turn ON/OFF)
Q_B & Q_S	Hard switching operation	Soft switching operation

Meanwhile, the proposed structure has a similar voltage stress on D_S as the conventional one as in (16) and (17) because D_S is located at the secondary side both in the conventional and proposed standby structures.

$$V_{DS-Conv}=V_{Link}/n+V_{STB}, \quad (16)$$

$$V_{DS-Pro}=V_{AC}/n+V_{STB}, \quad (17)$$

where $V_{DS\text{-}Conv}$ and $V_{DS\text{-}Pro}$ are voltage stresses on D_S in the conventional and proposed standby structures, respectively.

E. ZVS condition of Q_B

In the conventional boost PFC converter, the ZVS operation of Q_B cannot be achieved due to positive turn-on current of Q_B. Thus, the conventional boost PFC converter has a large turn-on switching loss and discharging loss of Q_B. However, as mentioned in Section II-B, i_{Llkg} of the proposed standby structure decreases considerably while delivering the power from the PFC stage to V_{STB} so it can have a negative direction. Thus, the proposed structure achieves a negative turn-on current of Q_B, which can be obtained by using (3), (10), and (11) as follows:

$$\begin{aligned} i_{QB-ON}&=i_{Llkg}(t_2)\\ &=i_{AC-Avg}-0.5\Delta i_{LB}-\frac{V_{Link}-V_{AC}-nV_{STB}}{L_{lkg}}(D_{STB}-D_X)T_S, \end{aligned} \quad (18)$$

where $i_{QB\text{-}ON}$ is the turn-on current of Q_B, $i_{AC\text{-}Avg}$ is the average input current, and Δi_{LB} is the ripple current of i_{LB}.

Therefore, provided that $i_{QB\text{-}ON}$ is a negative value, the ZVS operation of Q_B can be achieved by the energy stored in L_{lkg}. The ZVS condition of Q_B is expressed as follows:

$$L_{lkg}i_{QB-ON}^2\geq(C_{OSS-QB-ER}+C_{OSS-QS-ER})V_{Link}^2, \quad (19)$$

where $C_{OSS\text{-}ER}$ is the effective energy related output capacitance of $C_{OSS\text{-}QB}$ and $C_{OSS\text{-}QS}$.

In summary, based on parts A~E, the key differences between the conventional and proposed standby structures are summarized as shown in Table I. The proposed standby structure can increase the control complexity because it should synchronize the operation of Q_{STB} and Q_B. Moreover, it can be effective only in applications where the standby stage provides much lower output power than the PFC stage, such as server power supplies and PC power supplies. This is because higher output power of the standby stage causes much larger negative i_{Llkg}, which leads to larger conduction losses and larger EMI filter size compared to the conventional standby structure.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

TABLE II
DESIGN PARAMETERS OF PFC STAGES

Items	Conventional	Proposed
Boost switch, Q_B	IPP60R099C6 ($C_{OSS\text{-}QB\text{-}ER}$: 100pF)	
Rectifier switch, Q_S	GS66508T ($C_{OSS\text{-}QS\text{-}ER}$: 88pF)	IPP60R099C6 ($C_{OSS\text{-}QS\text{-}ER}$: 100pF)
Magnetic core	Boost inductor (L_B) Core : CH270043*2EA L_B : 610μH N_1 : 82T (1.0ϕ)	Boost transformer (T_{pro}) Core : CH270043*2EA L_B : 610μH, L_{lkg} : 35μH $N_1 : N_2$ = 82(1.0ϕ) : 24(0.8ϕ)

However, in the server power applications, since the standby output power is much smaller than the main output power, the side effect of the negative i_{Llkg} on the conduction loss and EMI filter can be negligible. Moreover, the proposed standby structure can eliminate the conventional flyback transformer (T_{Fly}) and RCD snubber, which results in high power density and high efficiency. Furthermore, it can reduce the switching losses on Q_{STB}, Q_B, and Q_S. Therefore, the proposed standby structure can achieve high efficiency and high power density compared to the conventional standby structure.

III. DESIGN CONSIDERATION OF PROPOSED STANDBY STRUCTURE

The proposed standby structure is composed of the proposed PFC and standby stages as shown in Fig. 4. Thus, we discuss each stage to explain the design consideration of the proposed standby structure in this section. The design specifications are 100-240V_{RMS} AC input (Nominal input: 115V_{RMS} and 230V_{RMS}), 750W PFC output, and 24W/12V standby output.

A. Proposed PFC stage

In (12), the voltage gain of the proposed PFC stage is the same as that of the conventional CCM boost PFC converter. Thus, the proposed PFC stage can be designed like the conventional CCM boost PFC converter, which is well described in [20]. Table II shows the designed parameters of the conventional and proposed PFC stages. From this table, in the conventional PFC stage, the GaN device is used for Q_S to relieve the reverse recovery problems. On the other hand, in the proposed PFC stage, the Si-MOSFET can be used for Q_S because the proposed PFC stage is able to alleviate the reverse recovery problems by obtaining the soft switching operation. The boost inductor (L_B) is designed to be about 610μH using two high-flux CH 270043 cores for 20% ripple current at 115V_{RMS} condition. Meanwhile, since the proposed PFC stage replaces L_B with a transformer (T_{Pro}), it has a leakage inductor (L_{lkg}) measured as 35μH in the experiment due to the secondary winding (N_2). Thus, the volume of T_{Pro} may be slightly larger than that of the conventional L_B due to N_2. However, the proposed PFC stage can be designed and controlled like the conventional CCM boost PFC converter because L_{lkg} is much smaller than L_B.

B. Proposed standby stage

In the proposed standby structure, since the standby stage shares the structure of the PFC stage, it should be designed not to have influence on the design procedure of the PFC stage.

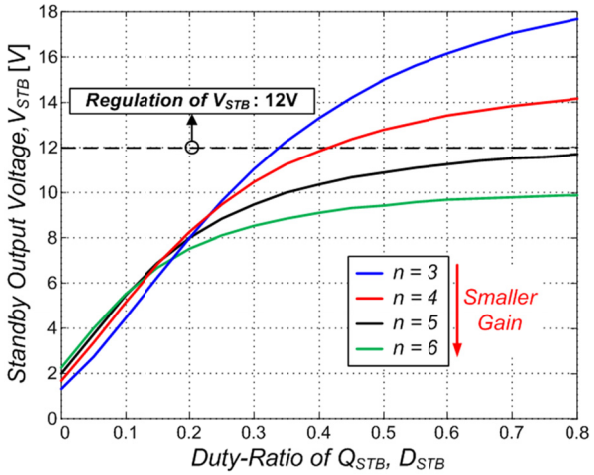

Fig. 8. V_{STB} of proposed standby stage according to D_{STB} and n at 264V_{RMS} condition.

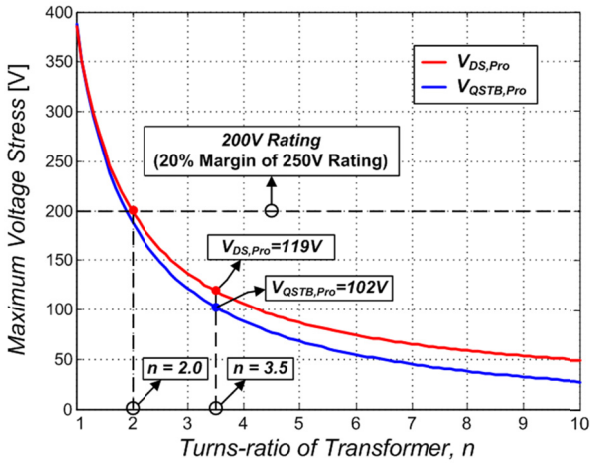

Fig. 9. Maximum voltage stress on Q_{STB} and D_S according to n.

Consequently, almost parameters of the proposed standby stage, such as V_{Link}, L_B, and L_{lkg}, are determined by the design procedure of the PFC stage. As a result, a design parameter of the proposed standby stage is the turns-ratio of T_{Pro} (n), which must properly be selected by considering following conditions: 1) voltage gain, 2) voltage stress, 3) ZVS condition of Q_B.

First, the voltage gain of the proposed standby stage should be taken into account. As mentioned previously, the worst input and output conditions of the proposed standby stage is the highest v_{AC} and largest $I_{O\text{-}STB}$. Moreover, in this example, a 10% voltage margin is considered. Thus, n should be designed at 264V_{RMS} input and 2A output current conditions. Fig. 8 shows V_{STB} of the proposed standby stage according to D_{STB} and n at 264V_{RMS} and full load conditions. As can be seen in Fig. 8, the maximum V_{STB} decreases as n increases. In particular, when n is larger than 5, the proposed standby stage cannot regulate V_{STB} as 12V regardless of D_{STB}. Therefore, n should be smaller than 5 to meet the voltage regulation requirement.

Second, the voltage stresses on Q_{STB} and D_S should be considered. In (15) and (17), the maximum $V_{QSTB\text{-}Pro}$ and $V_{DS\text{-}Pro}$ are depicted according to n, as shown in Fig. 9. From this figure, the maximum $V_{QSTB\text{-}Pro}$ and $V_{DS\text{-}Pro}$ increase when n decreases. Thus, n needs to be larger to use lower voltage rated

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

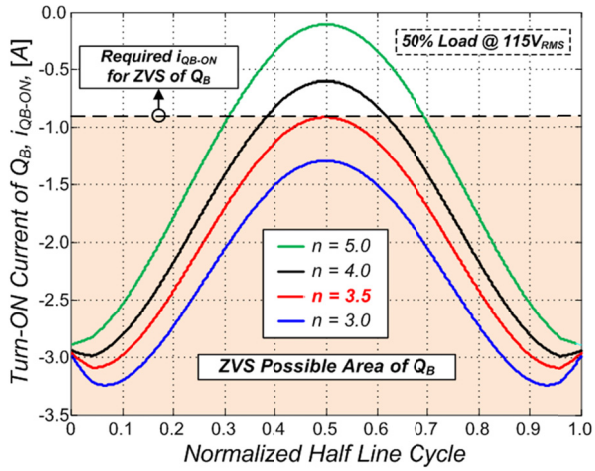

Fig. 10. Turn-on current of Q_B according to n at 115V_{RMS} and 50% load conditions.

semiconductor devices, which generally have a higher performance, such as a low channel-resistance and low forward voltage drop. In particular, considering a 20% voltage margin, n should be larger than 2 to adopt less than 250V rated semiconductor devices in this example.

Finally, n should be designed taking into account the ZVS condition of Q_B. As mentioned before, the proposed standby structure can have negative turn-on current of Q_B ($i_{QB\text{-}ON}$) as in (18). Thus, when n is designed to satisfy (19), the proposed standby structure achieves not only a zero reverse recovery of Q_S but also the ZVS operation of Q_B. Meanwhile, among load conditions, the server power supply should achieve the highest efficiency at 50% load conditions [2]. Moreover, between two nominal input voltage conditions, i.e., 115V_{RMS} and 230V_{RMS} conditions, it is difficult to achieve the ZVS operation at 115V_{RMS} conditions. Thus, the proposed standby structure is designed to achieve the ZVS operation at 115V_{RMS} and 50% load conditions in this example. Fig. 10 shows $i_{QB\text{-}ON}$ according to n at 115V_{RMS} and 50% load conditions. Moreover, based on design specifications and Table II, the required $i_{QB\text{-}ON}$ guaranteeing the ZVS operation of Q_B is depicted as the dashed line. Thus, the region below the dashed line means the ZVS possible area of Q_B. For example, when n is larger than 3.5, the proposed standby structure cannot satisfy the ZVS condition of Q_B around the peak of v_{AC}, which results in a turn-on switching loss and a discharging loss of Q_B. On the other hand, when n is smaller than 3.5, too much negative current flows through Q_B and Q_S. Thus, it causes a large conduction loss and turn-off switching loss of Q_B and Q_S.

In summary, n is selected as 3.5 in this example by considering the three conditions, i.e., voltage gain, voltage stress, and ZVS condition. Thus, $V_{QSTB\text{-}Pro}$ is 102V, $V_{DS\text{-}Pro}$ is 119V, and N_2 can be chosen as 24 turns.

IV. Experimental Results

To confirm the validity of the proposed standby structure, we built and tested a prototype with the specifications of 100-240V_{RMS} AC input (Nominal input: 115V_{RMS} and 230V_{RMS}), 750W PFC output, 24W/12V standby output, and 100kHz switching frequency. In addition, for the comparison, we also

Table III
Design Parameters of Standby Stages

Items	Conventional	Proposed
Switch, Q_B	SPA08N80C3 (V_{DS}=800V, R_{DS}=650mΩ)	IPI110N20N3G (V_{DS}=200V, R_{DS}=13mΩ)
Diode, Q_S	STPS20120C (V_{RRM}=120V, V_F=0.51V)	MBR20200CT (V_{RRM}=200V, V_F=0.63V))
Magnetic core	Core : EED1521 L_m : 1mH, L_{lkg}= 30μH N_1 : N_2 = 78 (0.25ϕ) : 10 (0.6ϕ)	-
RCD snubber	R_{snb} : 40kΩ, C_{snb} : 47nF D_{snb} : S1M(V_{RRM}=1200V)	-

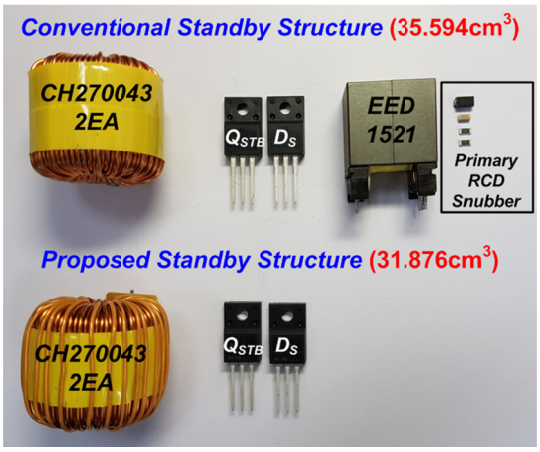

Fig. 11. Size comparison of key components.

implemented a prototype of the conventional standby structure. In two prototypes, Q_B and Q_S operate with the CCM duty ratio regardless of load conditions for high power quality by avoiding the input current distortion in the mixed conducted mode(MCM) [4], [21]. Moreover, a digital controller TMS320F28069 was used due to its flexibility, and the designed parameters are presented in Tables II and III. These tables show that the proposed PFC stage has the same parameters as the conventional boost PFC converter except for the secondary winding of T_{Pro}, which slightly increases the volume of T_{Pro} compared to the conventional L_B. On the other hand, in the standby stage, the proposed structure used Q_{STB} with a 200V rated device, which is much smaller than the conventional Q_{STB} with an 800V rated device. Moreover, it eliminates the large transformer and RCD snubber used in the conventional flyback converter. As a result, as shown in Fig. 11, the proposed standby structure reduces the total volume of key components so that it can achieve a higher power density than the conventional standby structure.

Figs. 12 and 13 show the experimental waveforms of the proposed standby structure under 10% and 100% load conditions at 115V_{RMS} and 230V_{RMS}, respectively. These figures show that i_{Llkg} of the proposed structure has a negative current direction, which is unlike the conventional boost PFC converter [3]-[5]. Thus, the proposed structure is able to achieve the soft switching operation of Q_B and Q_S. Moreover, despite a negative i_{Llkg}, since the input filter can average the input current (i_{AC}), the shape of i_{AC} is well controlled like v_{AC}. Therefore, the proposed structure maintains good power quality like the conventional boost PFC converter. Furthermore, V_{STB} is well regulated in the proposed structure.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

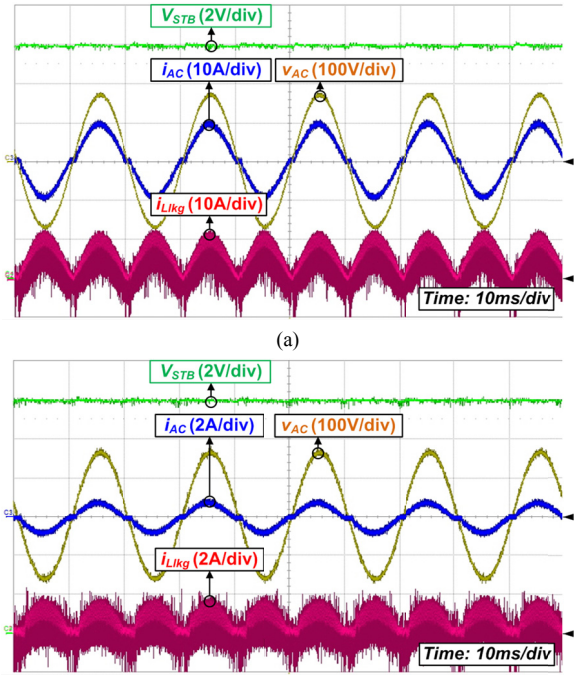

Fig. 12. Experimental key waveforms of proposed standby structure at $115V_{RMS}$. (a) 100% load condition. (b) 10% load condition.

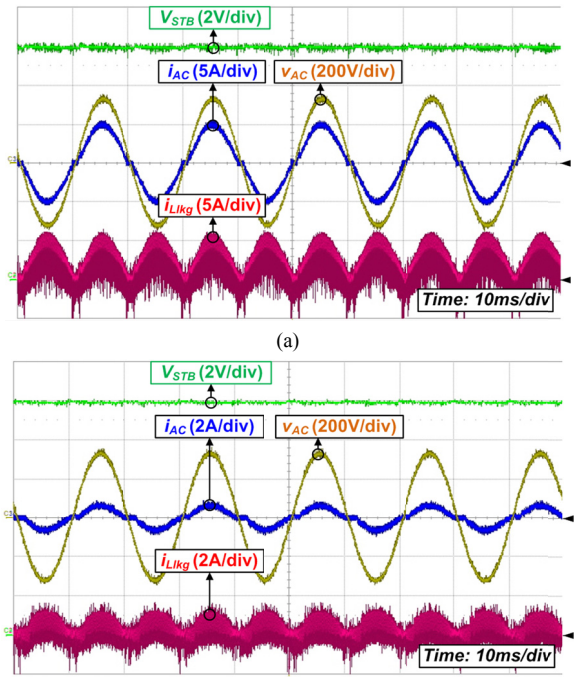

Fig. 13. Experimental key waveforms of proposed standby structure at $230V_{RMS}$. (a) 100% load condition. (b) 10% load condition.

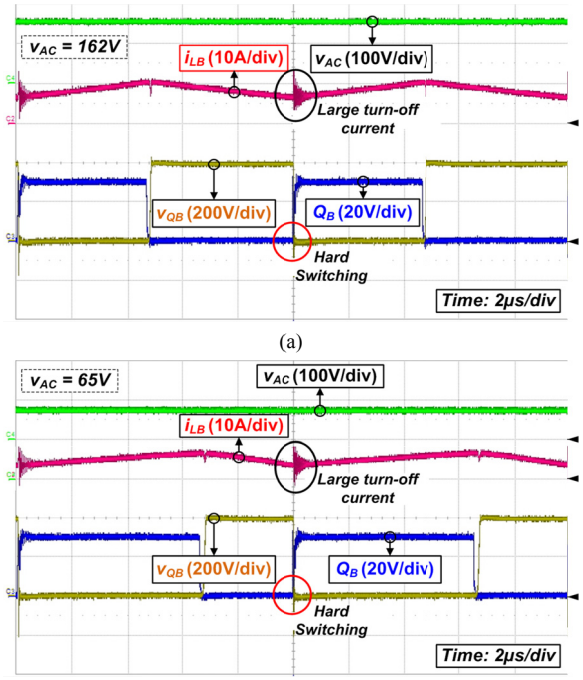

Fig. 14. ZVS waveforms of Q_B in conventional standby structure at $115V_{RMS}$ and 100% load conditions. (a) v_{AC}=162V. (b) v_{AC}=65V.

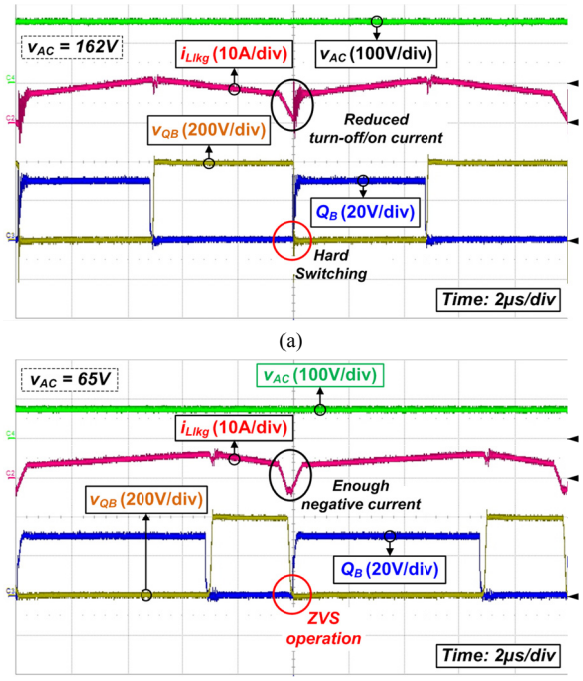

Fig. 15. ZVS waveforms of Q_B in proposed standby structure at $115V_{RMS}$ and 100% load conditions. (a) v_{AC}=162V. (b) v_{AC}=65V.

Fig. 14 shows the ZVS waveforms of Q_B in the conventional standby structure at $115V_{RMS}$ and 100% load conditions, which is the worst ZVS condition of Q_B between two nominal input conditions. From these figures, the boost inductor current (i_{LB}) has a positive current direction regardless of v_{AC}. Thus, Q_B and Q_S have the hard switching operation, which causes large switching loss and reverse recovery problems at the turn-on state of Q_B. On the other hand, Fig. 15 shows the ZVS waveforms of Q_B in the proposed standby structure. In Fig. 15(a), when v_{AC} is 162V, i_{Llkg} does not have a negative current because i_{AC} is larger than the transferred current into the standby stage. Thus, Q_B and Q_S

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

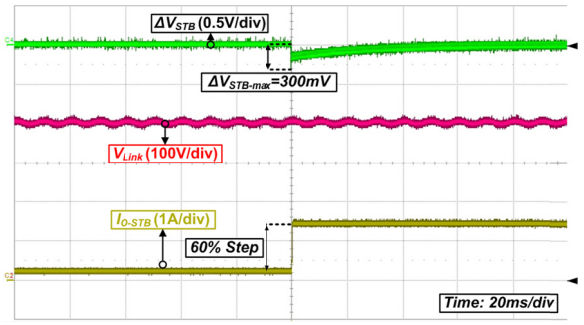

Fig. 16. Experimental waveforms with standby load transient from 10% to 70% at $230V_{RMS}$.

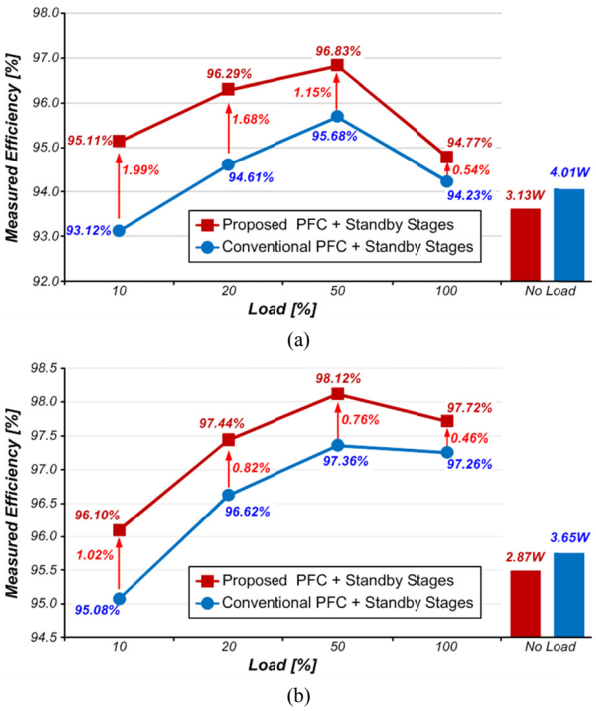

Fig. 17. Measured efficiency. (a) $115V_{RMS}$. (b) $230V_{RMS}$.

have the hard switching operation like the conventional boost PFC converter. However, since the turn-on and turn-off currents of Q_B and Q_S are considerably reduced, the turn-on switching loss of Q_B and reverse recovery problems are relieved compared to the conventional ones. On the other hand, in Fig. 15(b), when v_{AC} is lower than 65V, i_{Llkg} has enough negative current to achieve the ZVS operation of Q_B due to a small i_{AC}. Therefore, unlike the conventional boost PFC converter, the proposed structure achieves the soft switching operation of Q_B and Q_S, which results in a small switching loss.

Fig. 16 shows experimental waveforms with the standby load transient at $230V_{RMS}$ and 100% PFC output conditions. Since the proposed standby stage has similar characteristics with the DCM buck converter, it can achieve 10kHz bandwidth. Thus, despite of the 60% load variation, the standby output voltage is well regulated and varies within 600mV. Meanwhile, the proposed PFC stage can achieve similar dynamic performance with the conventional one because it is able to be designed like the conventional PFC stage.

Fig. 17 shows the measured system efficiency of the conventional and proposed standby structures at $115V_{RMS}$ and

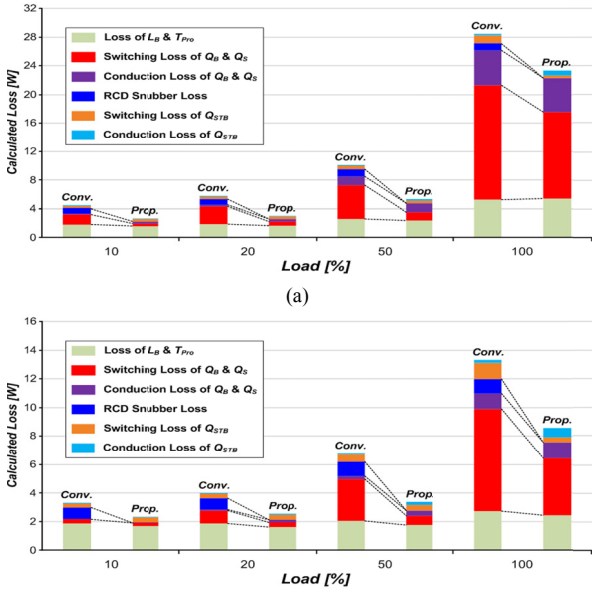

Fig. 18. Loss distribution. (a) $115V_{RMS}$. (b) $230V_{RMS}$.

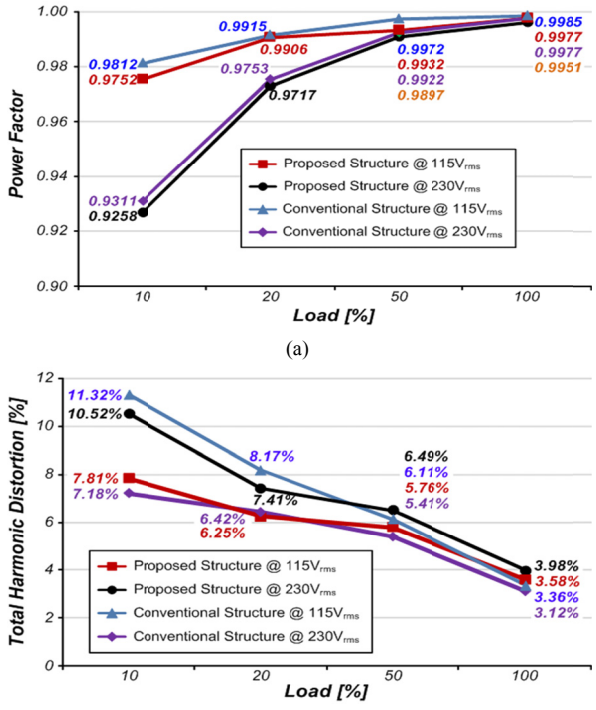

Fig. 19. Measured power quality. (a) $115V_{RMS}$. (b) $230V_{RMS}$.

$230V_{RMS}$ in the normal mode where the server power supply usually operates. Moreover, the efficiency was measured with two power analyzers, WT1600, to measure the input and output power. In this figure, the proposed standby structure has a higher efficiency than the conventional one over the entire load and input voltage conditions. This result is achieved by the eliminated RCD snubber loss and reduced switching loss of Q_B, Q_S, and Q_{STB}. In addition, at no-load condition, the proposed standby structure can achieve small no-load power consumption compared to the conventional standby structure because it can reduce the power loss caused

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

by the standby stage. The detailed loss distribution is shown in Fig. 18. In addition, as can be seen in Fig. 19, the proposed structure has a power factor (PF) and total harmonic distortion (THD) similar to the conventional standby structure. This is because it can be controlled like the conventional boost PFC converter and its input filter can make the impact of negative i_{Llkg} on the power quality be negligible. As a result, the proposed structure achieves not only higher efficiency but also higher power density than the conventional standby structure while maintaining high power quality.

V. Conclusion

In this paper, we proposed a new standby structure in which the primary side of the flyback converter is integrated with the boost PFC converter to improve the efficiency and power density of the server power supply. Compared to the conventional standby flyback converter, which suffers from high voltage stress and a large transformer, the proposed standby stage relieves high voltage stress and eliminates the large transformer. Thus, the proposed standby structure improves the efficiency and power density of the standby stage. Moreover, when the input power is transferred from the proposed PFC stage to the standby stage, the proposed PFC stage can obtain a negative current direction. Thus, the proposed PFC stage can obtain a soft switching operation of Q_B and Q_S, which leads to higher efficiency. As a result, the proposed standby structure is expected to be very attractive in a server power supply requiring high efficiency and high power density.

Reference

[1] Climates Savers Computing Initiative (CSCI) [Online]. Available: http://www.energystar.gov/

[2] *80 Plus Incentive Program* [Online]. Available : http://www.80plus.org/

[3] Y. S. Kim, W. Y. Sung, and B. K. Lee, "Comparative performance analysis of high density and efficiency PFC topologies," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2666-2679, Jun. 2014.

[4] H. S. Youn, J. S. Park, K. B. Park, J. I. Baek, and G. W. Moon, "A Digital Predictive Peak Current Control for Power Factor Correction With Low-Input Current Distortion," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 900-912, Jan. 2016.

[5] H. S. Youn, J. S. Park, K. B. Park, J. I. Baek, and G. W. Moon, "A Digital Predictive Peak Current Control for Power Factor Correction With Low-Input Current Distortion," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 900-912, Jan. 2016.

[6] Infineon, Munich, Germany, "20W Server Standby with ICE2A265", Design Note, Nov. 2001.

[7] Power Integrations, San Jose, CA, USA, "255W 80 PLUS Platinum PC Power Supply Using HiperPFS™-2PFS7328H and Hiper LCS™ LCS703HG," Design Example Report, Jan, 2014.

[8] Power Integrations, San Jose, CA, USA, "255W 80 PLUS Platinum PC Power Supply Using HiperPFS™-2PFS7328H and Hiper LCS™ LCS703HG," Design Example Report, Jan, 2014.

[9] J. K. Kim, S. W. Choi, C. E. Kim, and G. W. Moon, "A New Standby Structure Using Multi-Output Full-Bridge Converter Integrating Flyback Converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4763-4767, Oct. 2011.

[10] S. Y. Cho, I. O. Lee, J. K. Kim, and G. W. Moon, "A New Standby Structure Based on a Forward Converter Integrated With a Phase-Shift Full-Bridge Converter for Server Power Supplies," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 336-346, Jan. 2013.

[11] J. W. Kim, G. W. Moon, and I. O. Lee, "Standby-Loss Elimination in Server Power Supply," *Energies*, vol. 10, no. 7, pp. 981-994, July, 2017.

[12] J. Li, F. B. M. van Horck, B. J. Daniel, and H. J. Bergveld, "A High-Switching-Frequency Flyback Converter in Resonant Mode", *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8582-8592, Nov. 2017.

[13] K. B. Park, C. E. Kim, G. W. Moon, and M. J. Youn, "PWM Resonant Single-Switch Isolated Converter," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1876-1836, Aug. 2009.

[14] S. W. Lee and H. L. Do, "A Single-Switch AC-DC LED Driver Based on a Boost-Flyback PFC Converter With Lossless Snubber," *IEEE Trans. Power Electron.*, vol. 32 no. 2 pp. 1375-1384, Feb. 2017.

[15] A. B. Shitole, S. Sathyan, H. M. Suryawanshi, G. G. Talapur, and P. Chaturvedi, "Soft-Switched High Voltage Gain Boost-Integrated Flyback Converter Interfaced Single-Phase Grid-Tied Inverter for SPV Integration," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 482-493, Jan./Feb. 2018.

[16] Y. Jang, D. L. Dillman, and M. M. Jovanovic, "A New Soft-Switched PFC Boost Rectifier With Integrated Flyback Converter for Standby-by Power," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 66-72, Jan. 2006.

[17] J. Yang, "Efficiency Improvement with GaN-Based SSFET as Synchronous Rectifier in PFC Boost Converter," *in proc. PCIM Europe 2014*, pp. 1011-1016, May 2014.

[18] D. Han, C. T. Morris, W. K. Lee, B. Sarlioglu, "A Case Study on Common Mode Electromagnetic Interference Characteristics of GaN HEMT and Si MOSFET Power Converters for EV/HEVs", *IEEE Trans. Power Electron.*, vol. 3, no. 1, pp. 168-179, Mar. 2017.

[19] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics 2nd edition*: Kluwer Academic Publisher, 2001.

[20] S. Abedl-Rahman, "CCM PFC Boost Converter Design (DN 2013-01)." Infineon Technologies North America, Jan. 2013. [Online]. Available: http://www.infineon.com/

[21] K. D. Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche, J. A. Melkebeek, "Input-Current Distortion of CCM Boost PFC Converters Operated in DCM," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 858-865, Apr. 2007.

Jae-Il Baek (S'14-M'18) received the B.S. degree in the Electronics and Electrical Engineering from Sungkyunkwan University, Suwon, Korea in 2007, and the M.S. and Ph. D. degrees in the Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2015 and 2018.

He is currently working as a Postdoctoral Researcher at KPEL, KAIST, Daejeon, Korea. His research interests are in the areas of power electronics, particularly dc/dc converters, ac/dc converters, LED drivers, eco-friendly vehicles, and digital control approach of converters.

Jae-Kuk Kim (S'08-M'15**)** received the B.S. degree in the Electrical Engineering from Inha University, Incheon, Korea in 2004, and the M.S. and Ph.D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 2007 and 2011, respectively. From 2011 to 2015, he was a senior engineer in Samsung Electro-Mechanics, Suwon, Korea. He is currently an Assistant Professor in the department of Electrical Engineering, Inha University, Incheon, Korea. His research interests include converter topology design, soft-switching technique, display driving system, server power system, and battery charger system.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2018.2871138, IEEE Transactions on Power Electronics

Jae-Bum Lee (S'12-M'17) was born in Korea, in 1983. He received the B.S. degree in the Electrical Engineering from Korea University, Seoul, Korea in 2010 and the M.S. and Ph.D. degrees in the Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2012 and 2016, respectively. He is currently working as researcher in Korea Railroad Research Institute (KRRI), Uiwang, Korea.

His main research interests include high voltage/power transformer design, high efficiency AC/DC and DC/DC converters, and digital control method in high power vehicles such as electric vehicles and rolling stock.

Moo-Hyun Park (S'16) was born in South Korea in 1993. He received the B.S., M. S. degrees in the Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015, 2017, respectively. He is currently working toward the Ph.D. degree in KAIST.

His research interests include DC/DC converters, power-factor-correction AC/DC converters, and digital control for power converters.

Gun-Woo Moon (S'92-M'00) received the M.S. and Ph.D. degrees in Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, in 1992 and 1996, respectively. He is currently a Professor in the department of Electrical Engineering, KAIST.

His research interests include modeling, design and control of power converters, soft-switching power converters, resonant inverters, distributed power systems, power-factor correction, electric drive systems, driver circuits of plasma display panels, and flexible ac transmission systems. Dr. Moon is a member of the Korean Institute of Power Electronics (KIPE), Korean Institute of Electrical Engineers (KIEE), Korea Institute of Telematics and Electronics (KITE), Korea Institute of Illumination Electronics and Industrial Equipment (KIIEIE), and Society for Information Display (SID).